Edward Abban

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EDUCATION

University of California, Santa Cruz, Santa Cruz, CA — Expected Graduation: June 2030
Doctor of Philosophy in Computer Science and Engineering
Tufts University, Medford, MA
Bachelor of Science in Computer Engineering, GPA: 3.79
Awards: Morris and Sid Heyman Prize Scholarship**,** Dean Karno Scholar, Dean's List

EXPERIENCE

University of California, Santa Cruz — September 2025-Present
Research Assistant

- Benchmarked and profiled a ternary large language using Nvidia Nsight Compute on multiple platforms including Nvidia H100, Jetson Nano, and RTX 3090 ti

Tufts Computer Architecture Lab — September 2024–May 2025
Research Assistant

- Analyzed heatsink effectiveness on advanced hotspots on data center CPUs using Sniper, McPat, and 3D-ICE for performance, power and thermal modeling
- Refactored project code and updated three simulators for compatibility with RedHat 8, ensuring seamless migration from RedHat 6
- Wrote project documentation to streamline onboarding and increase usability

Amazon — June -September 2025
Software Development Intern

- Developed a service to allow echo devices to send and receive text messages and email on users phone's utilizing **C++** and bluetooth
- Implemented tests that allows for the simulation of different kinds of failure and dropout that occur from bluetooth

LinkedIn — May–September 2024
Software Engineering Intern

- Designed and implemented a high-performance file transfer service using **Golang** and **gRPC** to effectively transfer log files from 15,000+ network switches to monitoring servers. This significantly improved error visibility and provided valuable data for analysis
- Developed a user-friendly Command Line Interface (CLI) tool for retrieving and filtering log files from remote servers, enabling efficient time and network switch analysis.

PROJECTS

GShare Branch Predictor Simulation

- Created an accurate GShare branch predictor with configurable size and global history to simulate its impact on performance using the Sniper Multicore Simulator

ARMv8 5 Stage Pipelined Processor

- Implemented a 5-Stage pipelined CPU using **VHDL** that executes the **ARMv8** instruction set. Added hazard detection with stalling and forwarding to improve performance

CMOS Half Adder

- Designed and optimized a CMOS combinational binary counter using HSPICE, minimizing transistor count and worst-case delay through manual and automated optimization techniques.

SKILLS

- **Programming/Hardware Description Languages:** VHDL, Verilog, C, C++, Java, Rust, Golang, Python, Bash
- **Software Development Tools:** Git and GitHub, Linux, VS Code, SQL, Docker
- **Relevant Courses:** Computer Architecture, VLSI, Parallel Computing, Operating Systems

Memberships

National Society of Black Engineers, IEEE- Eta Kappa Nu